TITLE OF THE INVENTION

BIPOLAR TRANSISTOR

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a bipolar transistor, and particularly to a high-frequency silicon bipolar transistor.

(2) Description of the Related Art

In recent years, the mobile communication market is increasing with sophisticated, miniaturized and short-life devices. Further, cost effective transistors with flexible sizes are expected within a short period of time. As a means to meet these requirements, transistors of flexible transistor sizes are realized by setting up plural groups of transistors of required transistor sizes on one semiconductor substrate and connecting selected groups of transistors by lead wires. (For example, refer to Japanese Laid-Open Patent application No. 09-237882 (pp. 2-3, Fig. 7, Fig. 8).)

Hereinafter, a conventional bipolar transistor with a structure described above is explained using figures.

Figs. 1A and 1B are plan views of the top surface of the conventional bipolar transistor. Fig. 1A is a plan view when one group of transistors is selected; Fig. 1B is a plan view when two groups of transistors are selected.

As is shown in Figs. 1A and 1B, the conventional bipolar transistor is a comb-shaped and multi-fingered bipolar transistor in which unit transistors that compose a group or groups of transistors are connected in parallel. The conventional bipolar transistor is composed by connecting an emitter or emitters of a first group of transistors 110a and/or a second group of transistors 110b and/or a third group of transistors 110c with an emitter pad 140 for wire

bonding by an emitter lead wire 120 and connecting a base or bases of the first group of transistors 110a and/or the second group of transistors 110b and/or the third group of transistors 110c with a base pad 150 for wire bonding by a base lead wire 130. The first group of transistors 110a, the second group of transistors 110b and the third group of transistors 110c are formed on a predetermined area of a semiconductor substrate 100. Here, although it is not shown in Figs. 1A and 1B, a collector electrode is pulled out from the reverse side of the semiconductor substrate 100.

Here, the first group of transistors 110a, the second group of transistors 110b and the third group of transistors 110c are transistors in which a plurality of unit transistors with emitters, bases and collectors is connected electrically in parallel. Each group of transistors has a different number of unit transistors and the size of each group of transistors is different.

Fig. 2 is a cross-sectional view of the bipolar transistor (a cross-sectional view across the b-b' line in Fig. 1A). Note that the same elements in Fig. 1A are given the same characters and their detailed explanations are omitted here.

As is shown in Fig. 2, a plurality of unit transistors is formed in the first group of transistors 110a and the second group of transistors 110b. The plurality of unit transistors is composed of N type collectors 210 that are formed on an N^+ type semiconductor substrate 200 and that are made from silicon epitaxial layers, the P type bases 220 that are formed on the surface of the N type collectors 210 by an ion implantation technique, a silicon epitaxial method and the like, element separation regions 230 that are formed in the N type collectors 210 in order to insulate and separate each P type base 220, and N type emitters 240 that are formed on surfaces of the P type bases 220 by diffusing an impurity. In order to separate the first group of transistors 110a and the second group of transistors 110b completely like islands, an insulation separation

region 250 that is formed by a trench separation method, a LOCOS (Local Oxidation of Silicon) method and the like, and the depth of which reaches the N^+ type semiconductor substrate 200, is formed as a channel stopper between the first group of transistors 110a and the second group of transistors 110b. The plurality of unit transistors is covered by an insulation film 260.

Additionally, N type polycrystalline silicon films 270 are formed on the N type emitters 240; the P type polycrystalline silicon films 280, as an outside base layer, are formed on the P type bases 220 and the element separation regions 230.

Here, through holes 290 that penetrate the insulation film 260 are formed in the insulation film 260. The emitter lead wire 120 and the base lead wires 130 are connected with the N type polycrystalline silicon films 270 and the P type polycrystalline silicon films 280 respectively via the through holes 290 in which wiring plugs are embedded.

Regarding the bipolar transistor with the structure described above, bipolar transistors of different transistor sizes are, as is shown in Figs. 1A and 1B, realized by selecting an arbitrary group or arbitrary groups of transistors among the first group of transistors 110a, the second group of transistors 110b and the third group of transistors 110c and connecting the emitter lead wire 120 and the base lead wire 130 with the selected group(s) of transistors. Here, a manufacturing method for the bipolar transistor with the structure described above is realized within the range of ordinary micro fabrication technology and self-aligning technology.

As is described above, since the conventional bipolar transistor can realize bipolar transistors of different transistor sizes only with selection and connection by wiring, it is possible to realize a bipolar transistor that has excellent manufacturing efficiency and enables itself to be provided to the market in a brief period of time.

However, since it is little better than a plurality of transistor

groups of required transistor sizes is aligned on one semiconductor substrate in the conventional bipolar transistor, there is a problem that the number of transistor sizes to be realized is limited and therefore it is impossible to meet further requirement of the market for flexible transistor sizes.

Then, as is shown in Fig. 3, a plan view and Fig. 4, a cross-sectional view (a cross-sectional view across the c-c' line in Fig. 3, the plan view) a bipolar transistor having one or plural number of unit transistors, the number being any one of integers ranging from 1 to 30, can be realized by forming a plurality of the N type emitters 240, for example thirty of them, in one group of transistors surrounded by the insulation separation regions 250, selecting the arbitrary emitter(s) and base(s) among the emitters and the bases formed in the group of transistors, and connecting the emitter lead wire(s) and the base lead wire(s) with the selected emitter(s) and base(s). Therefore, as a method for realizing a bipolar transistor that meets the above-mentioned requirement, a method for selecting and connecting the emitter(s) and the base(s) in one group of transistors is expected. By a method like this, however, whole conjunction capacitance of the base(s) and the collector(s) immediately below the unused emitter(s) is added as parasitic capacitance and capacitance between the collector(s) and the base(s) increases. Therefore, a problem that high-frequency characteristics deteriorate occurs and it is impossible to realize a bipolar transistor that meets the above-mentioned requirement by this method.

Moreover, as is shown in Fig. 5, a cross-sectional view, a bipolar transistor having one or plural number of unit transistors, the number being any one of integers ranging from 1 to 30, can be realized by forming a group of transistors whose number of emitters is one in a region surrounded by the insulation separation regions 250 on the same semiconductor substrate and setting up the plural

groups of transistors, for example thirty of them. Therefore, as a method for realizing a bipolar transistor that meets the above-mentioned requirement, a method for setting up the plural groups of transistors whose number of emitters is one is also expected. By a method like this, however, a base and a collector are independently formed for each emitter. Consequently, the problem that high-frequency characteristics deteriorate does not occur because the parasitic capacity does not become large but another problem occurs, the problem being that an extremely large semiconductor substrate is necessary because the insulation separation regions 250 exist among each group of transistors. For that reason, it is impossible to realize a bipolar transistor that meets the above-mentioned requirement by this method, either.

SUMMARY OF THE INVENTION

In view of the foregoing, it is the object of the present invention to provide a bipolar transistor that can meet requirement of the market for flexible transistor sizes.

To achieve the above-mentioned object, the bipolar transistor according to the present invention is (Claim 1).

Hereby, since the number of unit transistors for each group of transistors is 2^n (2, 4, 8, 16, $\cdots$), it is possible to realize the bipolar transistor having 2^n (i.e. all the even numbers to be realized) pieces of transistors, in other words, the bipolar transistor having various transistor sizes by selecting and connecting a plurality of groups of transistors. Therefore, an effect to realize the bipolar transistor that can meet requirement of the market for flexible transistor sizes is achieved.

Additionally, it is acceptable that (Claim 2). Here, the m may be 4.

Hereby, since the bipolar transistor includes a group of transistors that has every even number of unit transistors, the

number being 2 at the minimum and 2^m at the maximum, an effect to realize the bipolar transistor that has successive number of unit transistors is achieved.

Moreover, it is satisfactory that (Claim 4). Here, (Claim 5). Furthermore, it is acceptable that (Claim 6).

Hereby, since the connection among the selected groups of transistors is performed by the lead wires, an effect of realizing the bipolar transistor that enables transistor sizes to be changed easily is achieved.

Additionally, it is satisfactory that (Claim 7).

Hereby, an effect of realizing the bipolar transistor that has all the transistor sizes is achieved.

As further information about technical background to this application, Japanese patent application No. 2002-298761 filed on October 10, 2002 is incorporated herein by reference.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other subjects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings that illustrate a specific embodiment of the invention. In the Drawings:

Fig. 1A is a plan view of the top surface of the conventional bipolar transistor when one group of transistors is selected.

Fig. 1B is a plan view of the top surface of the conventional bipolar transistor when two groups of transistors are selected.

Fig. 2 is a cross-sectional view of the conventional bipolar transistor (a cross-sectional view across the b-b' line in Fig. 1A).

Fig. 3 is a plan view of the top surface of a modified example of the conventional bipolar transistor.

Fig. 4 is a cross-sectional view of a modified example of the conventional bipolar transistor (a cross-sectional view across the c-c' line in Fig. 3).

Fig. 5 is a cross-sectional view of another modified example of the conventional bipolar transistor.

Fig. 6 is a plan view of the top surface of the bipolar transistor according to the embodiment of the present invention.

Fig. 7 is an enlarged plan view of the bipolar transistor according to the embodiment of the present invention (an enlarged view of the Part A in Fig. 6).

Fig. 8 is an enlarged plan view of the bipolar transistor according to the embodiment of the present invention (an enlarged view of the first group of transistors 610a and the second group of transistors 610b).

Fig. 9 is a cross-sectional view of the bipolar transistor according to the embodiment of the present invention (a cross-sectional view across the d-d' line in Fig. 8).

Fig. 10 is a plan view of a modified example of the bipolar transistor according to the embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

The bipolar transistor according to the embodiment of the present invention will be explained below with reference to the figures.

Figs. 6-7 are plan views of the top surface of the bipolar transistor according to the embodiment of the present invention. Fig. 7 is an enlarged plan view of the Part A in Fig. 6.

As is shown in Fig. 6, the bipolar transistor according to the present embodiment is a comb-shaped and multi-fingered bipolar transistor that aims to realize a bipolar transistor which can meet requirement of the market for flexible transistor sizes and that is composed by connecting an emitter pad 640 for wire bonding via an emitter lead wire 620 with an emitter or emitters of a first group of transistors 610a and/or a second group of transistors 610b and/or a third group of transistors 610c and/or a fourth group of transistors

610d that are formed in a predetermined area on a semiconductor substrate 600 and connecting a base pad 650 for wire bonding via a base lead wire 630 with a base or bases of the first group of transistors 610a and/or the second group of transistors 610b and/or the third group of transistors 610c and/or the fourth group of transistors 610d.

Here, although it is not shown in Fig. 6, a collector electrode is pulled out from the reverse side of the semiconductor substrate 600. It is not, however, limited to this way.

Here, the first group of transistors 610a, the second group of transistors 610b, the third group 610c and the fourth group of transistors 610d are transistors in which a plurality of unit transistors having emitters, bases and collectors is connected electrically in parallel. The number of unit transistors of each group of transistors is different from each other, the number being 2^n (n is a positive integer) and 2 at the minimum and 2^m (m is the total number of the groups of transistors) at the maximum. By the way, when the bipolar transistor has groups of transistors that include 2, 4, 8 and 16 pieces of unit transistors, it is possible to pass a current of 100mA at the maximum in a tip area that causes no problem. Therefore, in the present embodiment, as Fig. 7 shows, the number of unit transistors of the first group of transistors 610a, the second group of transistors 610b, the third group of transistors 610c and the fourth group of transistors are decided to be 2, 4, 8 and 16, respectively.

Fig. 8 is an enlarged plan view of the first group of transistors 610a and the second group of transistors 610b in Fig. 7. Fig. 9 is a cross-sectional view of the bipolar transistor (a cross-sectional view across the d-d' line in Fig. 8). Note that the same elements in Fig. 6 as in Figs. 8-9 are given the same characters and their detailed explanations are omitted here.

As is shown in Figs. 8-9, a plurality of unit transistors is

formed in the first group of transistors 610a and the second group of transistors 610b. The plurality of unit transistors is composed of N type collectors 910 that are formed on an N^+ type semiconductor substrate 900 and that are made from silicon epitaxial layers, P type bases 920 that are formed on the surface of the N type collectors 910 by an ion implantation technique, a silicon epitaxial method and the like, element separation regions 930 that are formed in the N type collectors 910 in order to insulate and separate each P type base 920, and N type emitters 940 that are formed on surfaces of the P type bases 920 by diffusing an impurity. In order to separate the first group of transistors 610a and the second group of transistors 610b completely like islands, an insulation separation region 950 that is formed by a trench separation method, a LOCOS (Local Oxidation of Silicon) method and the like, and the depth of which reaches the N^+ type semiconductor substrate 900, is formed as a channel stopper between the first group of transistors 610a and the second group of transistors 610b. The plurality of unit transistors is covered by an insulation film 960. In addition, it is stated that the P type bases 920 are formed by an epitaxial method and the N type emitters 940 are formed by diffusing an impurity. But it is acceptable that the P type bases 920 and the N type emitters 940 are formed on the N type collectors 910 in sequence by epitaxial growth. Additionally, it is also acceptable that the P type bases 920 and the N type emitters 940 are formed on the surface of the N type collectors 910 in sequence by diffusing an impurity.

Moreover, N type polycrystalline silicon films 970 are formed on the N type emitters 940; P type polycrystalline silicon films 980, as outer base layers, are formed on the P type bases 920 and the element separation regions 930.

Here, through holes 990 that penetrate the insulation film 960 are formed in the insulation film 960. The emitter lead wires 620 and the base lead wires 630 are connected with the N type

polycrystalline silicon films 970 and the P type polycrystalline silicon films 980 respectively via the through holes 990 in which wiring plugs are embedded.

Regarding the bipolar transistor with the structure described above, bipolar transistors of different transistor sizes are, as is shown in Figs. 8 and 9, realized by selecting an arbitrary group or arbitrary groups of transistors among the first group of transistors 610a, the second group of transistors 610b, the third group of transistors 610c and the fourth group of transistors 610d and connecting the emitter lead wire 620 and the base lead wire 630 with the selected group(s) of transistors. Here, a manufacturing method for the bipolar transistor with the structure described above is realized within the range of ordinary micro fabrication technology and self-aligning technology.

As is described above, according to the present embodiment, the bipolar transistor includes the first group of transistors 610a, the second group of transistors 610b, the third group of transistors 610c and the fourth group of transistors 610d; the number of unit transistors is 2, 4, 8 and 16, respectively. Therefore, by changing combinations of the groups of transistors selected using the emitter lead wire 620 and the base lead wire 630, it is possible to realize the bipolar transistor having the even number of transistors, the number being any even number ranging from 2 to 30. Consequently, the bipolar transistor according to the present embodiment can realize the bipolar transistor that can meet the requirement of the market for flexible transistor sizes.

Furthermore, according to the present embodiment, it is not the emitter(s) and the base(s) but the group(s) of transistors that are selected. Therefore, in the selected group(s) of transistors, all the N type emitters 940 and all the P type bases 920 are used and the capacity among the collector(s) and the bases does not increase. Consequently, the bipolar transistor according to the present

embodiment can realize the bipolar transistor that does not deteriorate the high frequency characteristics.

Additionally, according to the present embodiment, the number of unit transistors of each group of transistors is different from each other, the number being 2^n and 2 at the minimum and 2^m at the maximum. Therefore, when compared with the case of setting up a plurality of transistors with one emitter, the number of the insulation separation regions that exist among the groups of bipolar transistors decreases. Consequently, the bipolar transistor according to the present embodiment can realize the bipolar transistor that does not need a large semiconductor substrate.

By the way, according to the present embodiment, it is stated that the bipolar transistor includes the group(s) of transistors that have 2^n, 2 at the minimum and 2^m at the maximum, pieces of unit transistors. The number of unit transistors is not, however, limited to 2^n when dimensional precision in manufacturing the unit transistors is not considered. As is shown in Fig. 10, a plan view, it is acceptable that the bipolar transistor further includes another group of transistors 610e whose number of the unit transistors is 1 and an arbitrary group or groups are selected from a plurality of groups of transistors including the group of transistors 610e.

Moreover, the emitter lead wire 620 and the base lead wire 630 are formed by one-layer lead wires but two-layer lead wires are also acceptable.

As is apparent from the description above, since the bipolar transistor according to the present embodiment can realize the bipolar transistor having every even number of unit transistors, the number being 2 at the minimum and 2^m at the maximum, an effect of realizing the bipolar transistor that has successive number of unit transistors and that can meet requirement of the market for flexible transistor sizes is achieved. Furthermore, since the bipolar transistor according to the present embodiment uses all the N type

emitters and P type bases in the selected group(s) of transistors, the capacity among the collector(s) and the bases does not increase. Therefore an effect of realizing the bipolar transistor that does not deteriorate the high-frequency characteristics is achieved. Additionally, the bipolar transistor according to the present embodiment has the fewer number of insulation separation regions that exist among each group of transistors when compared with the case of setting up a plurality of transistors with one emitter. Therefore, an effect of realizing the bipolar transistor that does not need a large semiconductor substrate is achieved.

Consequently, it is possible to provide the bipolar transistor that meets requirement of the market for flexible transistor sizes and its practical value is extremely high.